

FIG. 1

FIG. 2A is a block diagram of a network architecture. The architecture includes a plurality of network processors (202, 204, 206, ..., 208) connected to a plurality of VQM (Virtual Queue Manager) blocks (208, 210, 212, ..., 214). Each network processor is connected to its corresponding VQM block via a bidirectional connection (220, 222, 224, ..., 226). The VQM blocks are connected to a central switch (232) via a bus (230). The switch is connected to a plurality of CSW (Control Switch) blocks (214, 216, 218, ..., 220) via a bus (232). The CSW blocks are connected to a plurality of output ports (224, 226, 228, ..., 230) via a bus (232).

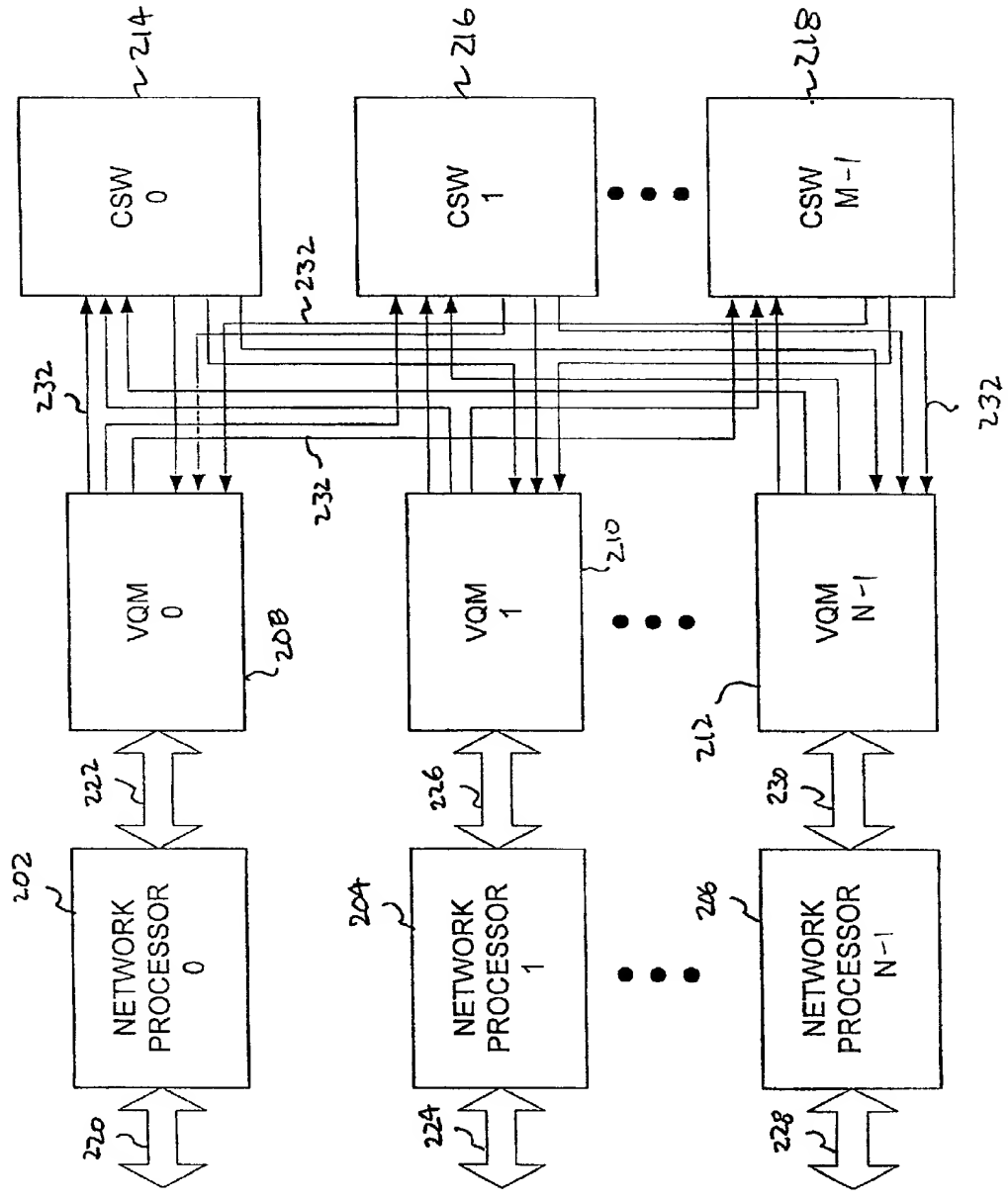


FIG. 2A

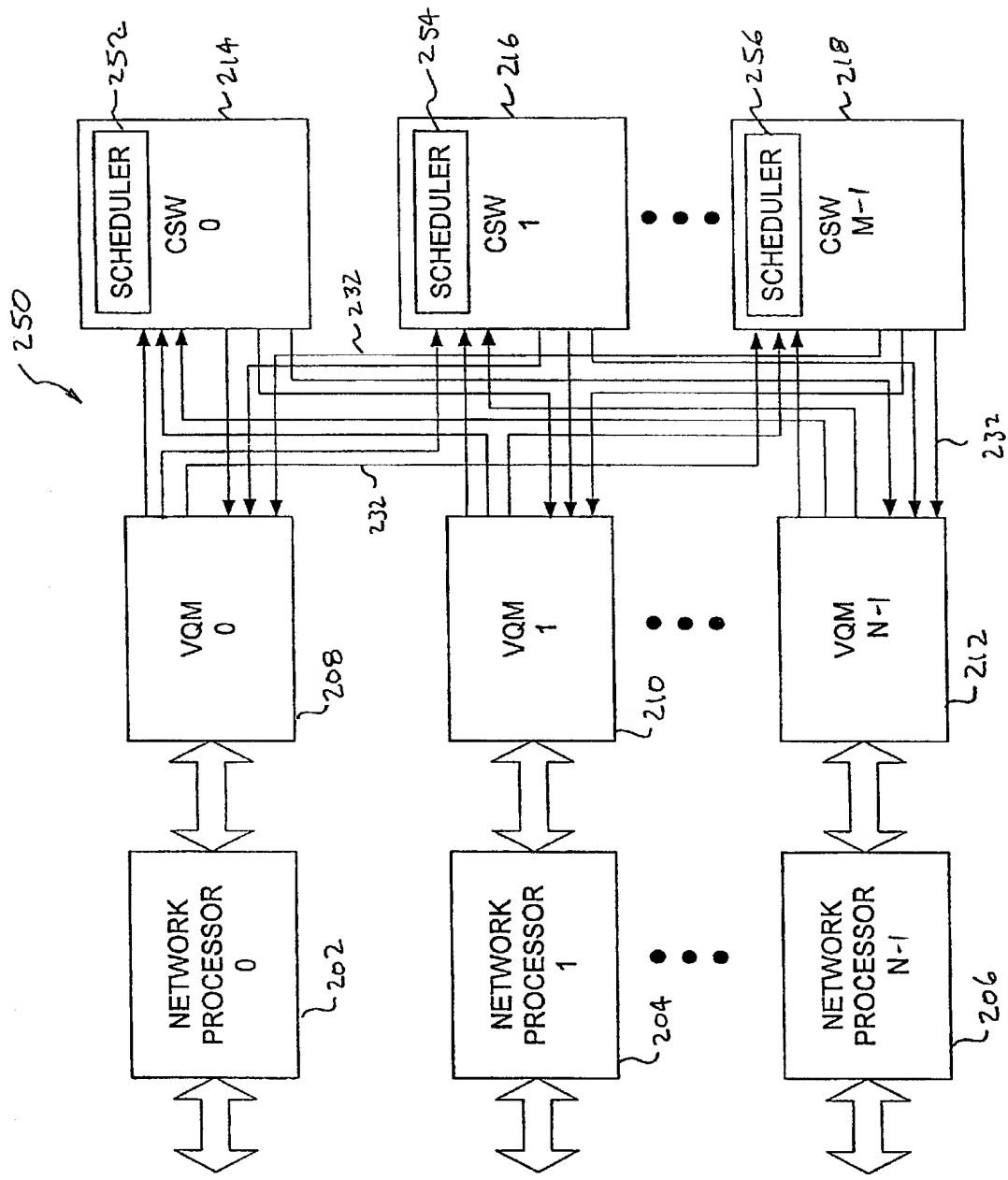


FIG. 2B

FIG. 2C

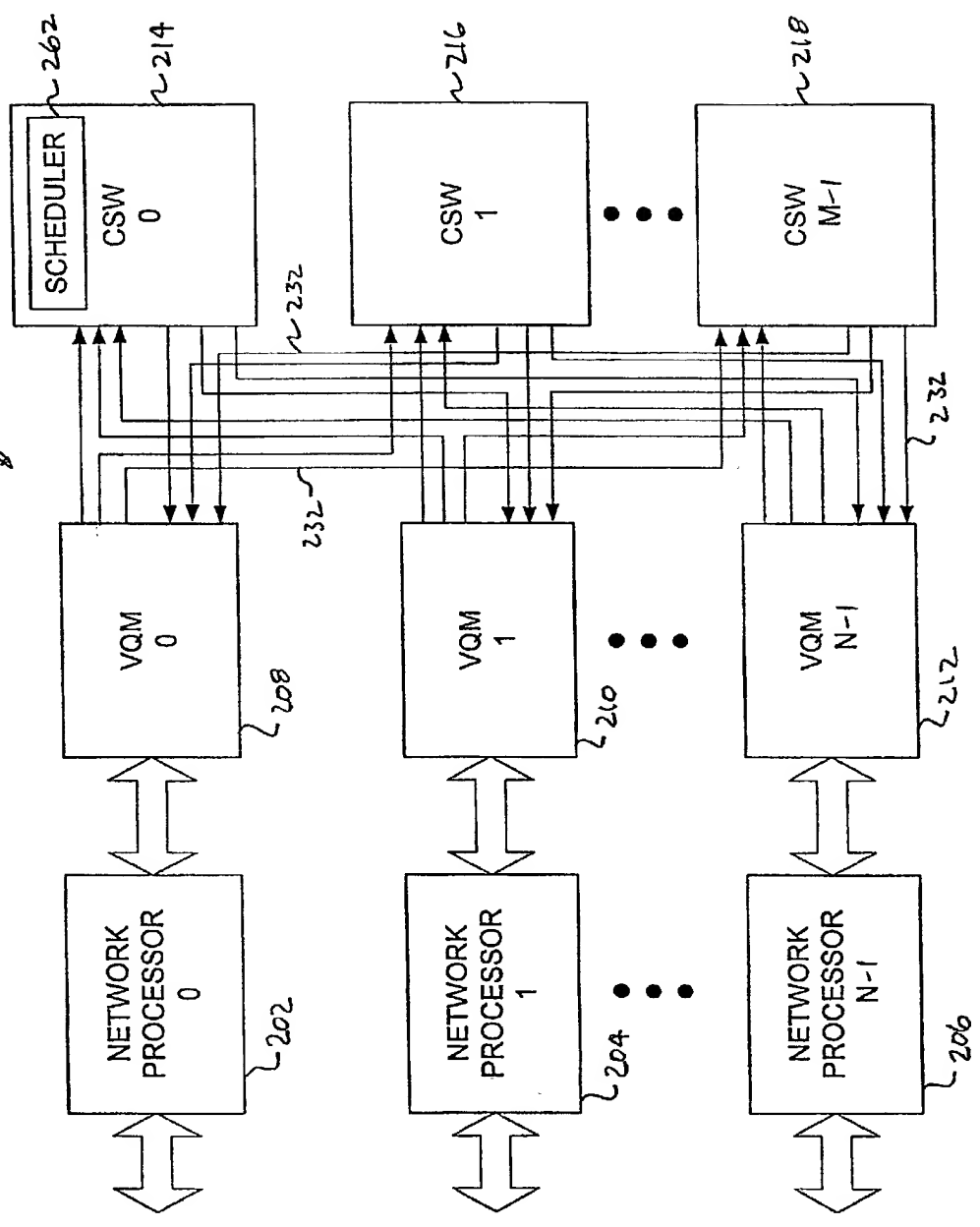


FIG. 2C

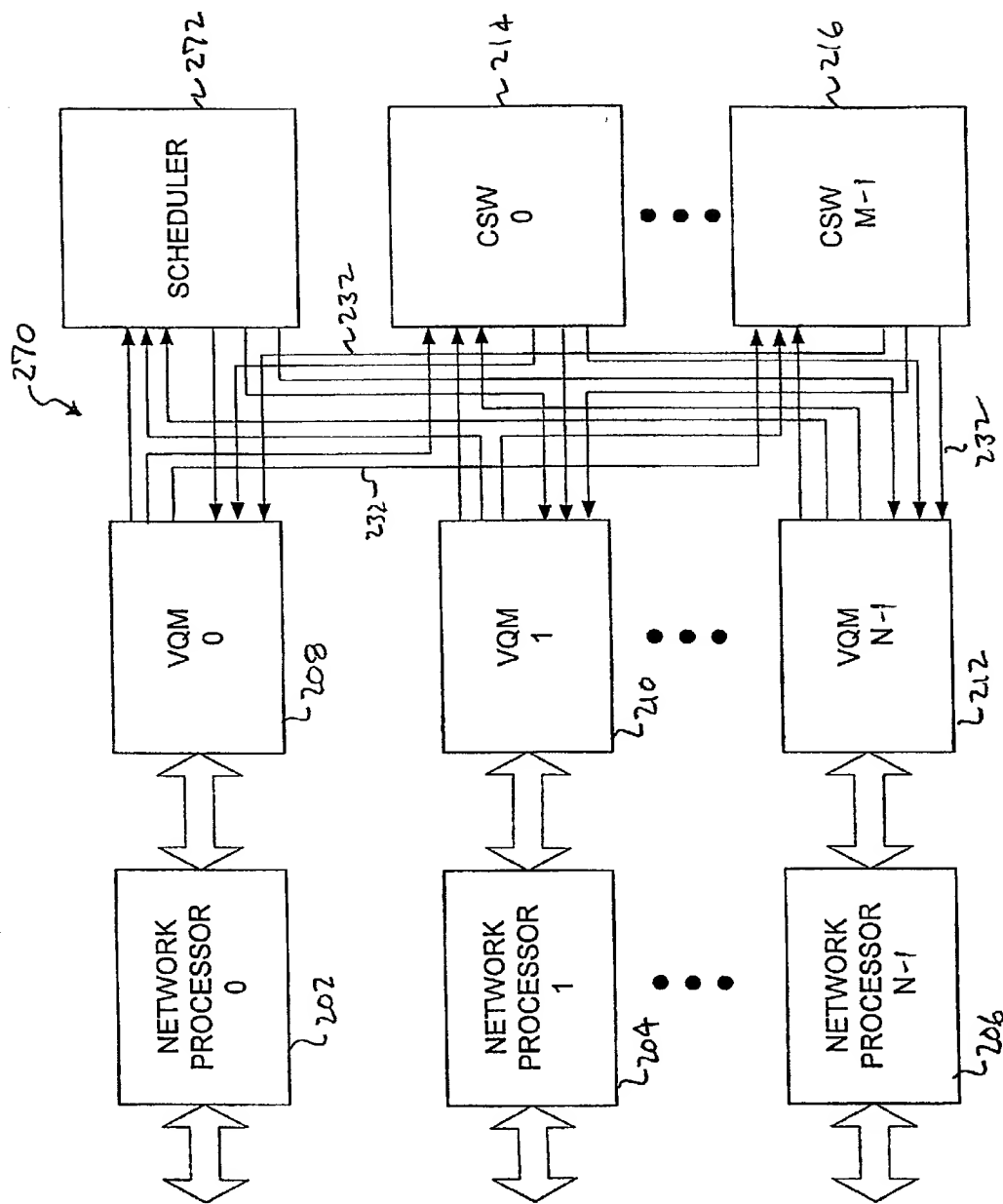


FIG. 2D

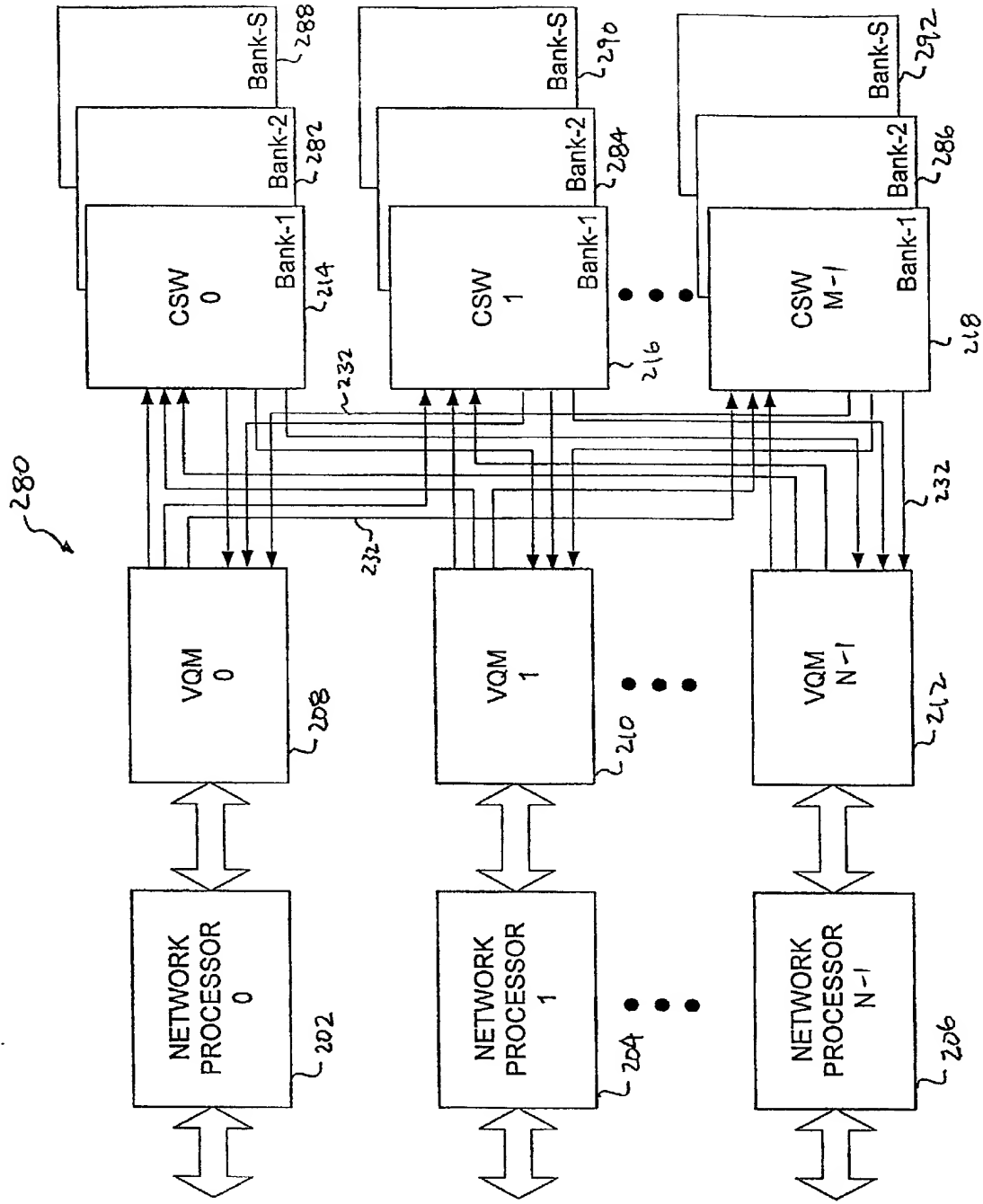


FIG. 2E

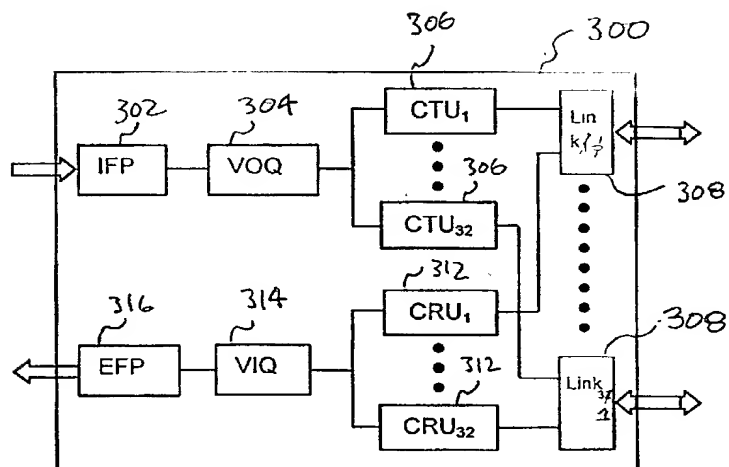


FIG. 3 [VQM]

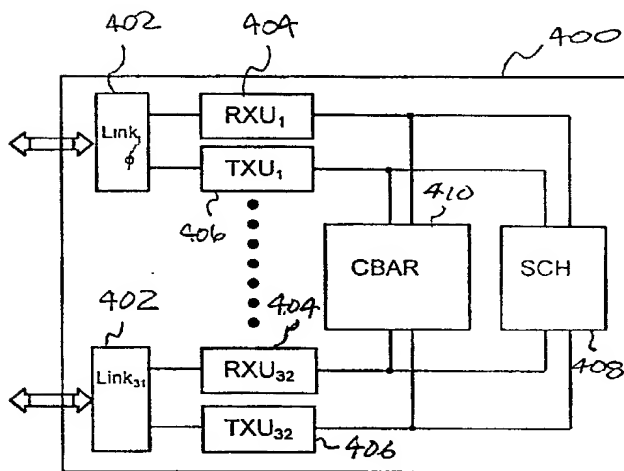


FIG. 4 [CSW]

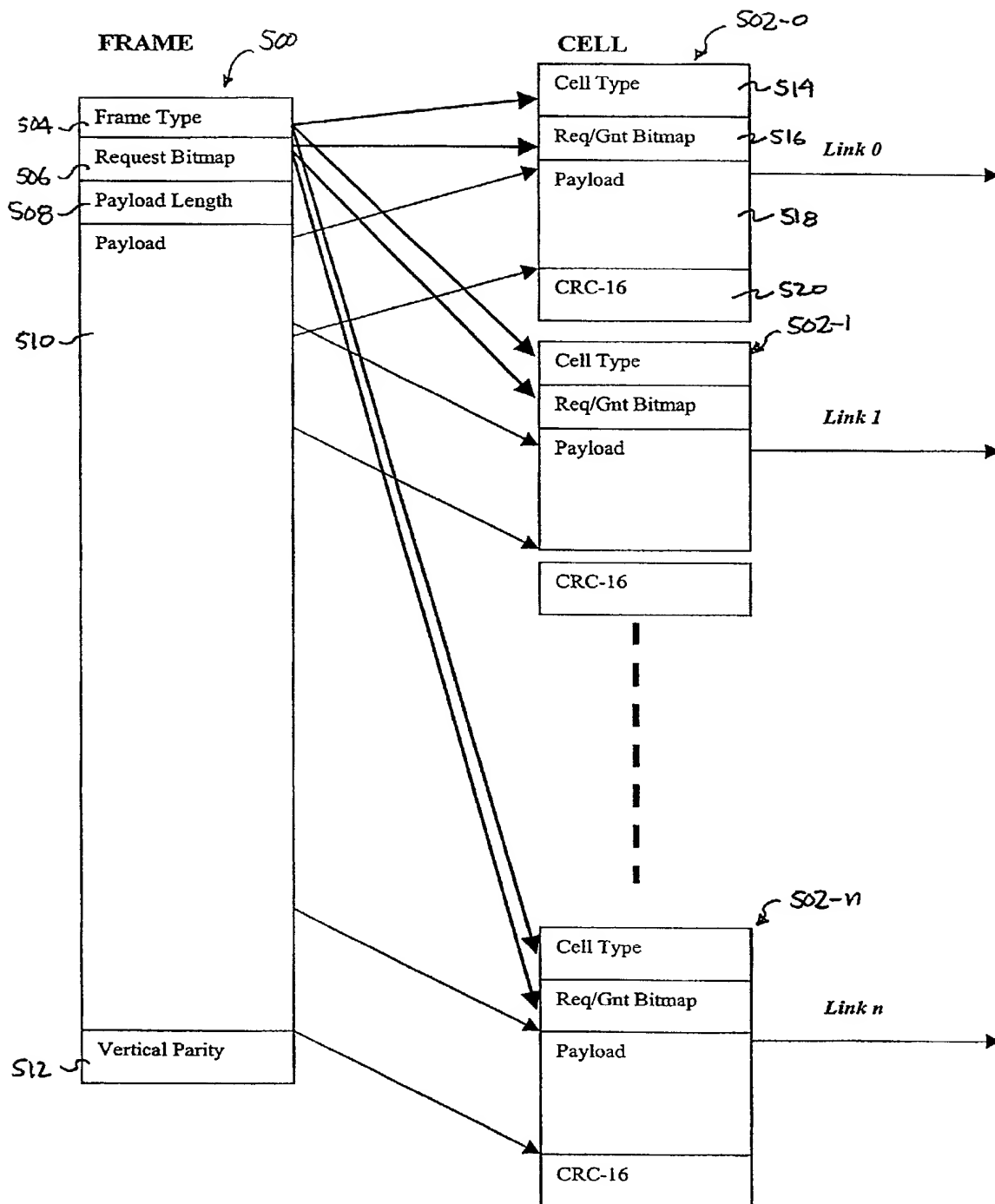


FIG. 5



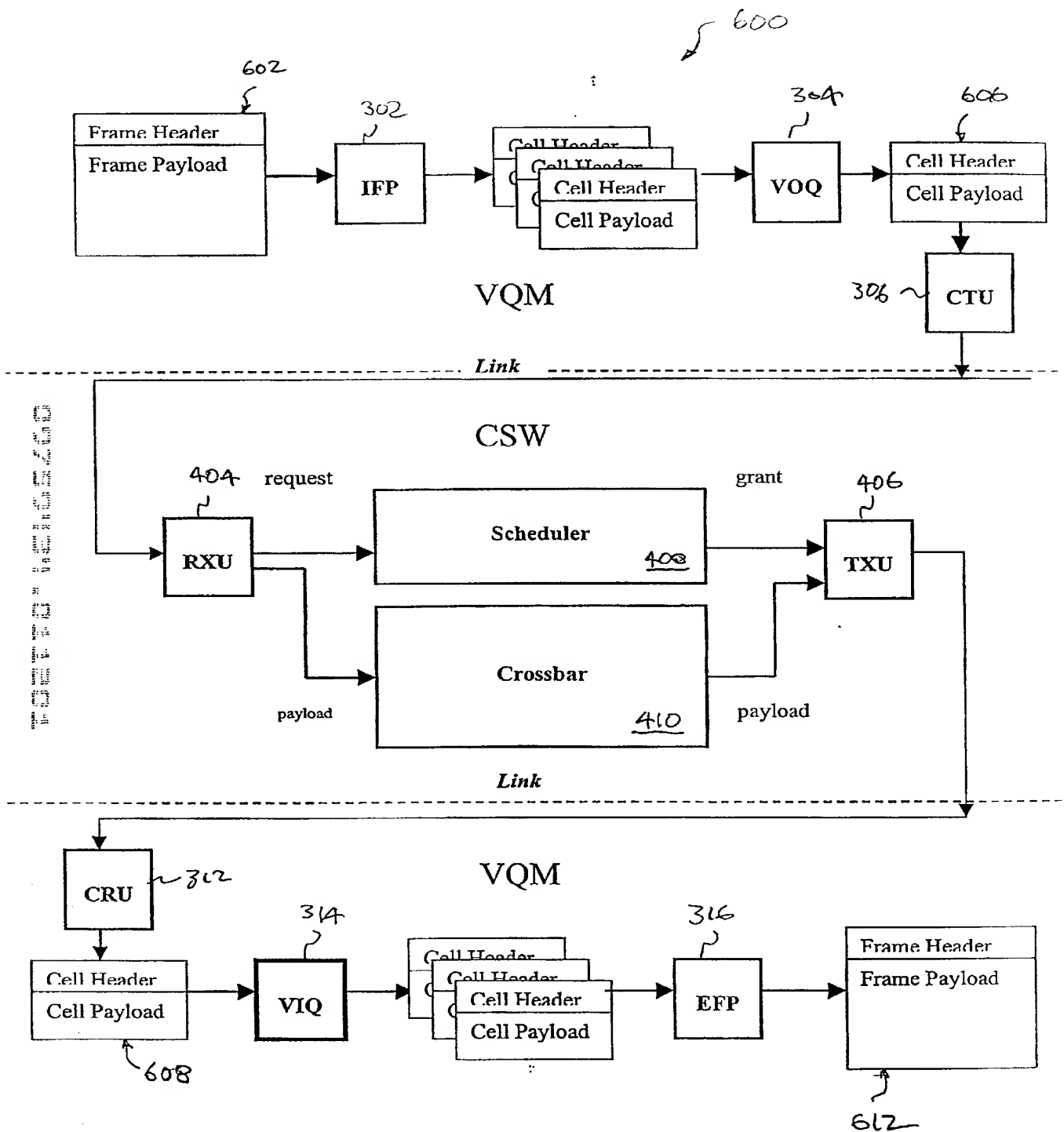


FIG. 6

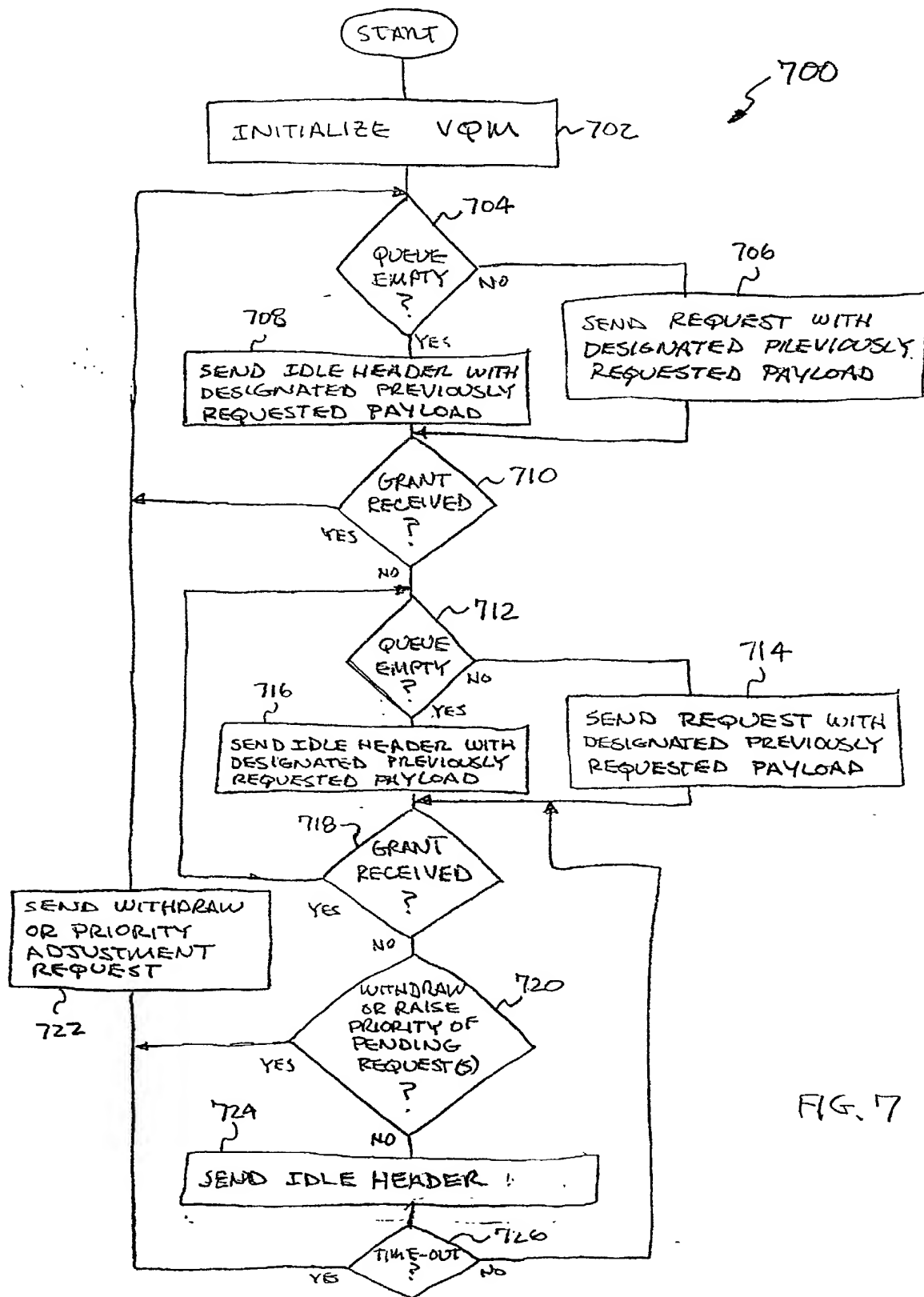


FIG. 7

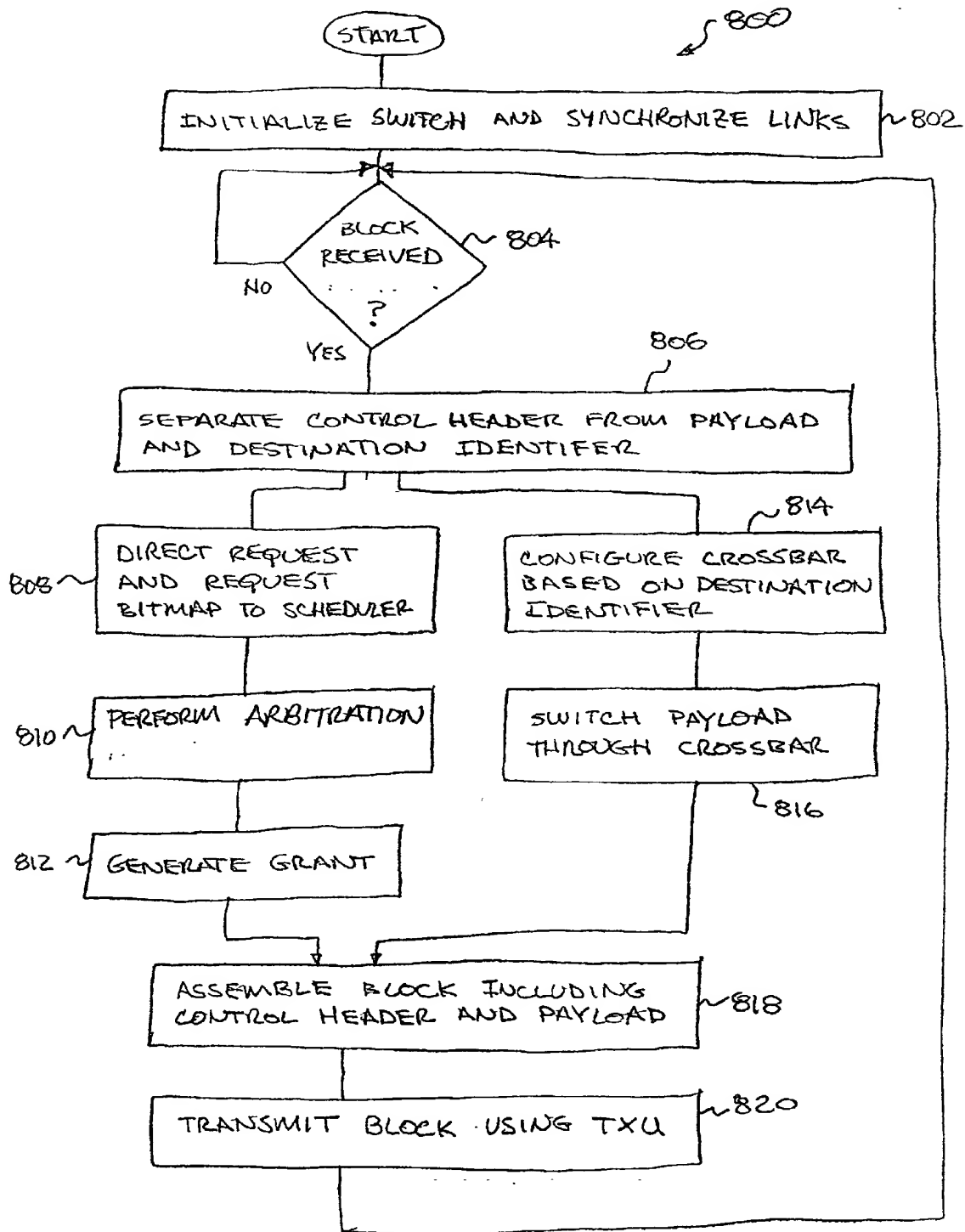


FIG. 8